Question [1]: [25 mark]

a) Using a suitable decoder and 3 logic gates, design a logic circuit that adds two 2-bit numbers, $N_1=A_1A_0$ and $N2=B_1B_0$, Where N_1 is the MS and N_2 is the LS. Carry in is zero (no carry in) (for example $N_1=10$, $N_2=11$, $N_1+N_2=101=C_{out}S_2S_1$, C_{out}=Carry out=1, S_2=Sum2=0, S_1=Sum1=1) (Hint: Construct the truth table to find the logic expressions of C_{out}, S_2 and S_1 in decimal minterms notation, then design the required circuit)

b) Design a circuit for C_{out} using multiplexer and some logic gates as required. Use A_1 and A_0 as select inputs.

Q1) Test 2

a)

A_1	A_0	B_1	B_0	C_0	S_2	S_1
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

3

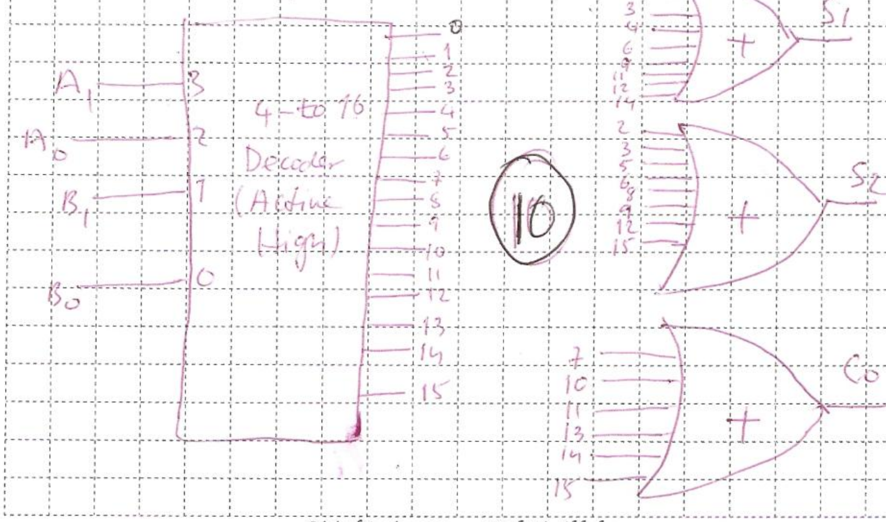
$S_1 = \Sigma m(1,3,4,6,9,11,12,14)$

$S_2 = \Sigma(2,3,5,6,8,9,12,15)$

$C_0 = \Sigma(7,10,11,13,14,15)$

2

A.S.A. Dr. Wael
This is the solution of Q1 -
M.A



b)

$$C_o = \sum m(7, 10, 11, 13, 14, 15)$$

B_1B_0 \ A_1A_0	I_0 00	I_1 01	I_3 11	I_2 10
00	0	0	0	0
01	0	0	1	0
11	0	1	1	1
10	0	0	1	1

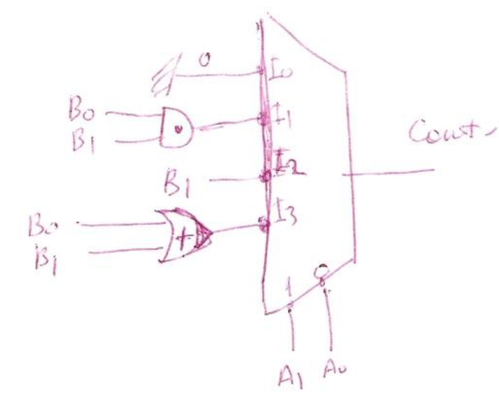
$I_0 = 0$

$I_1 = B_0B_1$

$I_2 = B_1$

$I_3 = B_0 + B_1$

10



Question [2]: [25 marks]

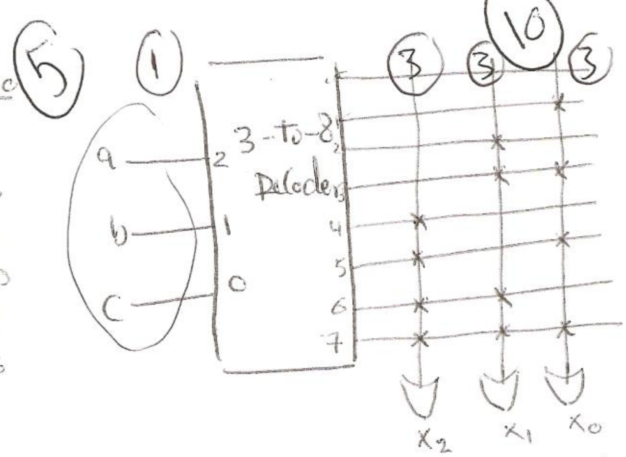
a. Realize the following set of Boolean equations using ROM implementation:

$$x_0(a,b,c) = c$$
$$x_1(a,b,c) = b$$
$$x_2(a,b,c) = a$$

Tabulate the truth table for the ROM, and then draw the circuit implementation of the ROM, and show the fuse mapping. **[15 marks]**

a	b	c	X_2	X_1	X_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

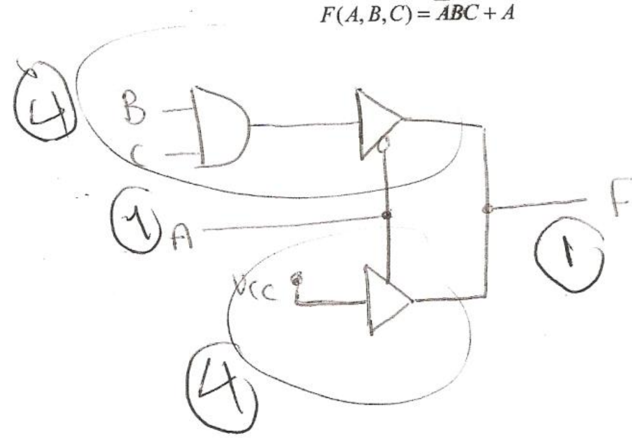
Truth Table for the RoM



RoM Cir Cuit Implementation

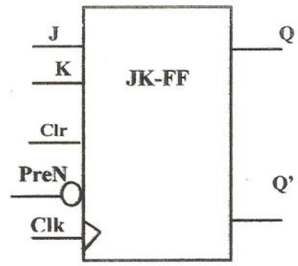
a. Realize the following function using three state buffers and any additional logic gates, and use A as a control signal: **[10 marks]**

$$F(A,B,C) = \overline{A}BC + A$$



Question [3]: [25 mark]

a. The JK-FF module given in figure (1) with a rising edge of the clock "clk", asynchronous active high "clear", and asynchronous active low "PreN". The output for JK-FF is Q. Figure (2) gives some forces for the inputs, Sketch the outputs Q, and consider a time delay for all changes in the output. **[15 marks]**



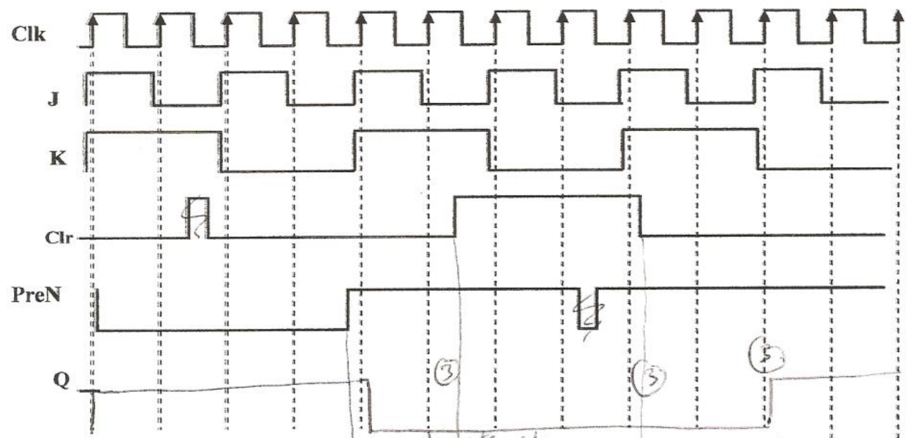
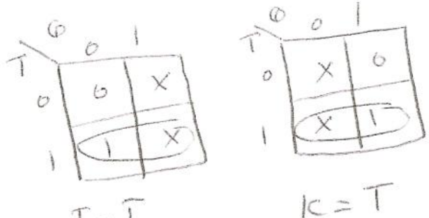


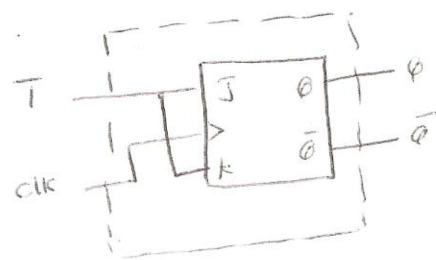
Figure (2)

a. Explain how to convert a single J-K-flip flop to T-flip flop. Show all of your steps. Draw the converted J-K flip flop with any additional gates. **[10 marks]**

Q	Q+	J	K	T
0	0	0	X	0
0	1	1	X	1
1	0	X	1	1
1	1	X	0	0



J = T (3) K = T (3)



(4)

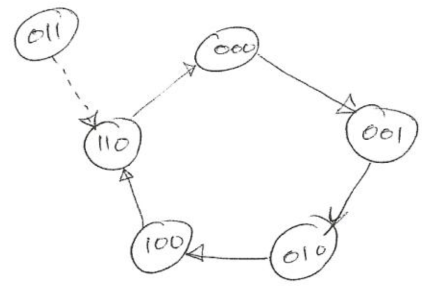
Question [4]: [25 mark]

Using falling-edge triggered D flip-flops, design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6.

a) Draw the logic diagram of the counter

b) What will happen if the counter is started in state 011.

C	B	A	C^+	B^+	A^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	–	–	–
1	0	0	1	1	0
1	0	1	–	–	–
1	1	0	0	0	0
1	1	1	–	–	–



BA \ C	0	1
00	0	1
01	0	X
11	X	X
10	1	0

BA \ C	0	1
00	0	1
01	1	X
11	X	X
10	0	0

BA \ C	0	1
00	1	0
01	0	X
11	X	X
10	0	0

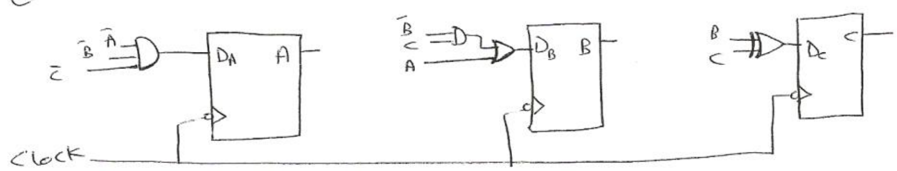
$D_C = C^+ = \bar{B}C + B\bar{C}$

$= B \oplus C$

$D_B = B^+ = \bar{B}C + A$

$D_A = A^+ = \bar{A}\bar{B}\bar{C}$

(a)



(b)